



Evaluation of SiC VJFET Devices for Scalable Solid-State Circuit Breakers

by Damian P. Urciuoli

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14. ABSTRACT Power electronic converters functioning as components in high power systems, such as those of hybrid military ground vehicles require fast fault isolation, and in most cases benefit additionally from bi-directional fault isolation. To prevent converter damage or failure, fault current interrupt speeds in the hundreds of microseconds to few millisecond range are necessary. Presently used mechanical contactors do not provide adequate actuation speeds, and suffer severe degradation during repeated fault isolation. Instead, it is desired to use a large array of semiconductor devices having a collectively low conduction loss to provide large current handling capability and fast transition speed for current interruption. This report discusses the use of SiC MOSFETs and the evaluation of SiC JFETs for a bi-directional solid-state circuit breaker application.					
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Introduction

Power electronic converters functioning as components in high power systems, such as those of hybrid military ground vehicles require fast fault isolation, and in most cases benefit additionally from bi-directional fault isolation. To prevent converter damage or failure, fault current interrupt speeds in the hundreds of microseconds to few millisecond range are necessary. Presently used mechanical contactors do not provide adequate actuation speeds, and suffer severe degradation during repeated fault isolation. Instead, it is desired to use a large array of semiconductor devices having a collectively low conduction loss to provide large current handling capability and fast transition speed for current interruption. The collector-to-emitter saturation voltage of IGBT devices results in large conduction losses for continuous currents, making IGBTs poor candidates for this application. Furthermore, neither IGBTs nor MOSFETs are optimized for reverse conduction, and have no inherent means of reverse voltage blocking.

Investigation Using MOSFETS

In a meeting with Jim Richmond and Bob Callanan of Cree, Inc. at the Army Research Laboratory (ARL) in early FY07, both suggested developing a solid-state contactor for protection of a non-isolated DC-DC converter. Their initial plan was to investigate the development of a solid-state contactor designed with silicon carbide (SiC) MOSFETs placed in parallel. On September 11, 2007, they both returned to ARL, when Bob Callanan discussed his progress on designing a control circuit for the contactor, including provision for precharging internal converter capacitance. He also mentioned the large number of 20 A rated SiC MOSFET die that would need to be placed in parallel to handle in excess of 500 A of current with the desired 1 V conduction drop across the part. ARL personnel mentioned that the large number of die would be necessary because a contactor power dissipation exceeding 500 W would provide significant thermal management challenges.

On September 12, 2007, the simplified ARL bi-directional converter schematic was sketched with the proposed MOSFET based contactor represented by a single MOSFET. It was then realized that the MOSFET body-diode would not provide converter protection for current in the reverse direction (buck mode operation of the converter). The converter schematic with MOSFET based contactor is shown in figure 1.

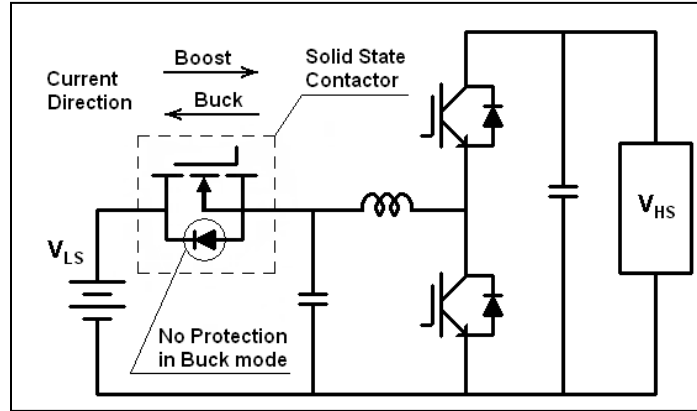


Figure 1. Bi-directional converter schematic with parallel MOSFET based solid-state contactor.

To behave like a mechanical contactor by stopping current flow in both directions, the MOSFET based contactor would require an additional set of paralleled MOSFETS placed in series with, but in the opposite direction of, the original set (back-to-back MOSFETS) with the source terminal of the MOSFETS connected together. This added set of MOSFETS would effectively double both the number of devices needed, and the amount of contactor loss compared to original estimates. The back-to-back MOSFET structure has been implemented in silicon for several low current applications and is shown in figure 2.

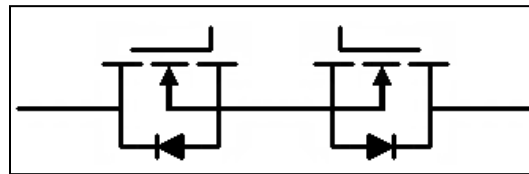


Figure 2. Back-to-back MOSFET structure having bi-directional current blocking.

Investigation Using Parallel SiC JFETs

The SiC JFET was considered as a possible candidate for use instead of a MOSFET in the design of a solid-state contactor. In this application a normally-on JFET would provide operation as a circuit breaker, interrupting current when actuated, much like fault protection provided by circuit breakers in utility power systems. Due to the lack of a parasitic body diode between the drain and source terminals of the JFET, it was suggested that a single device may be capable of bi-directional current conduction and bi-directional voltage blocking. It was hoped that with multiple devices connected only in parallel, and by not needing another set of devices to block

reverse current flow, conduction drop, and therefore losses, could be significantly reduced. Furthermore, many JFETs have lower conduction losses than comparably rated MOSFETs.

A bi-directional snubber was designed to reduce solid-state breaker voltage stress during fault isolation. Figure 3 shows the bi-directional snubber placed across the proposed JFET based breaker in the simplified bi-directional converter schematic. Simulations were conducted to determine suitable component ratings based on estimated worst case line inductances.

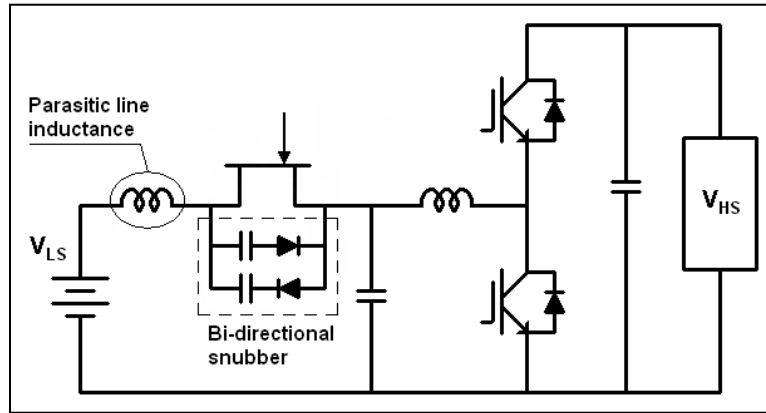


Figure 3. Bi-directional snubber design for solid-state breaker.

Northrop Grumman Corporation (NGC) has developed SiC normally-on vertical JFETs (VJFET) having current ratings of 20 A and 50 A with respective blocking voltages as high as 1900 V and 1200 V. Smaller 8 A rated sample VJFET parts were obtained for scaled down application testing. An isolated driver was designed and built to provide an adjustable gate-to-source (V_{GS}) bias of nominally +2 V for VJFET conduction, and an adjustable V_{GS} bias down to -24 V for blocking conditions. The driver was tested successfully on a small capacitive gate load.

Prior to delivery to ARL, 8 A chips were packaged, and individual negative and positive V_{GS} versus I_{GS} curves, V_{DS} versus I_{DS} *forward* blocking (blocking positive V_{DS}) curves, and V_{DS} versus I_{DS} *forward* conduction (positive current entering the drain and exiting the source) curves were characterized by NGC. Examples of each of these curves are shown in figure 4.

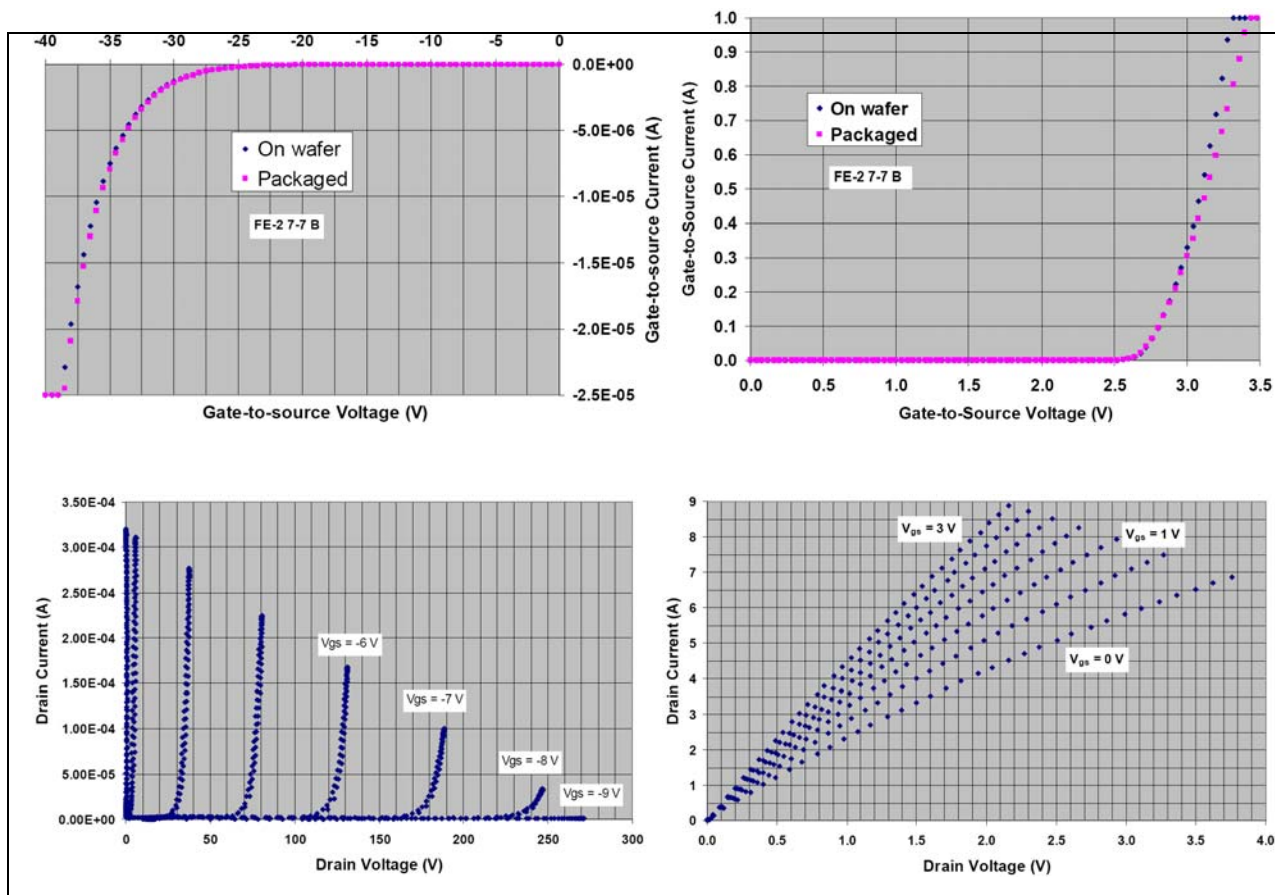


Figure 4. Negative V_{GS} versus I_{GS} (top left), Positive V_{GS} versus I_{GS} (top right), Forward blocking V_{DS} versus I_{DS} (bottom left), and Forward conduction V_{DS} versus I_{DS} (bottom right).¹

An absolute minimum V_{GS} value for the parts of -30 V is suggested to avoid part damage from source-to-gate breakdown. Under positive gate bias, a maximum V_{GS} of $+2.5$ V is suggested to avoid forward conduction of the parasitic diode that exists between the gate and source. The devices are capable of blocking V_{DS} well in excess of 300 V over the full negative range of V_{GS} , with V_{DS} limited to 300 V for un-potted parts. For a positive gate bias of 2 V, and an I_{DS} of 8 A, V_{DS} was measured at 2.3 V for the device with characteristics shown in figure 4. This corresponds to an on-state resistance of less than 0.3 ohms at full rated current. ARL personnel also requested that NGC evaluate: device *reverse* conduction (positive current entering the source and exiting the drain), forward current sharing between two devices, and reverse current sharing between two devices. Results for two 20 A VJFET parts are shown in figures 5 and 6. Although the devices share current well in both directions, the on-state resistance during reverse conduction is 15% to 20% higher than that for forward conduction.

¹ Figures 4, 5, and 6 are data provided by Northrop Grumman Corporation.

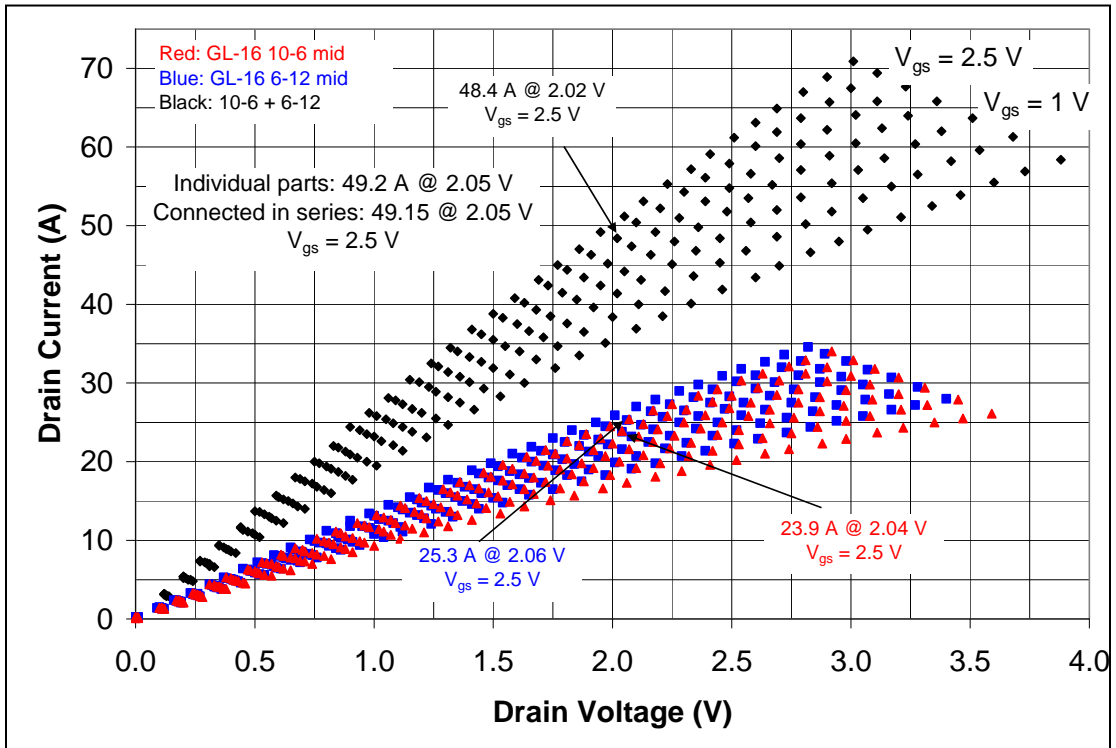


Figure 5. Individual and sharing forward conduction curves for two 20 A VJFETs.¹

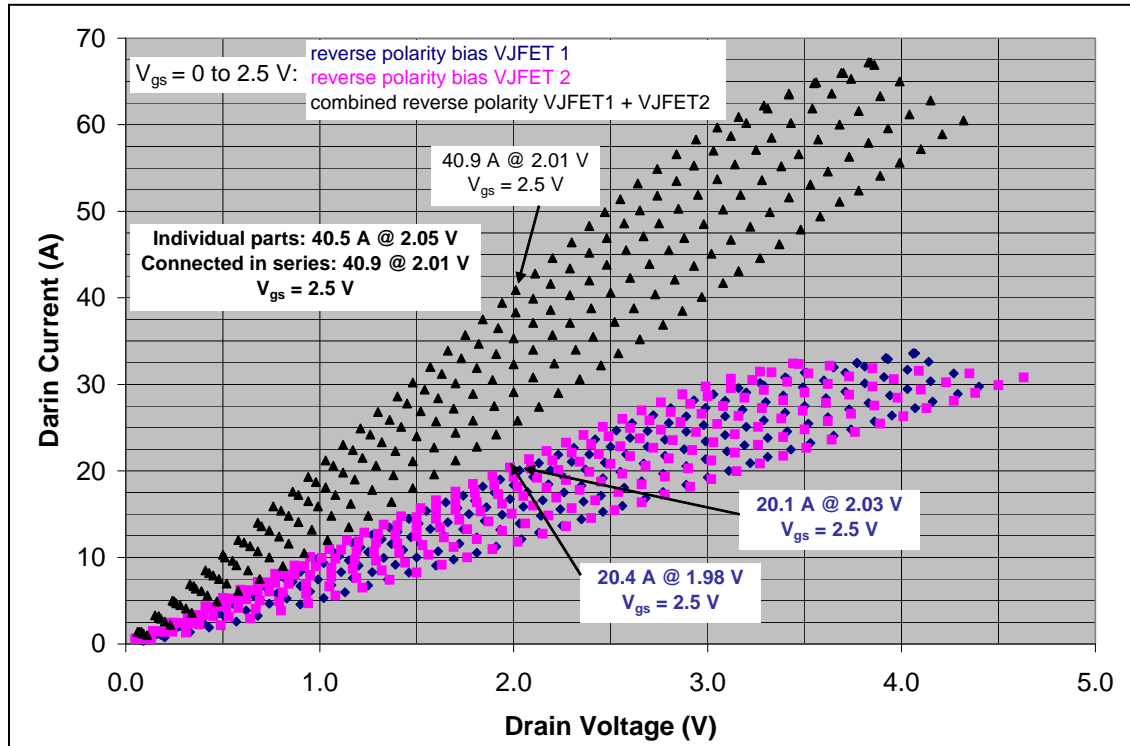


Figure 6. Individual and shared reverse conduction curves for two 20 A VJFETs (above).¹

The increase in on-state resistance during reverse conduction is believed to be common to the NGC VJFET device structure. During further technical discussions with NGC, ARL personnel discovered that the VJFET would not provide *reverse* blocking (blocking negative V_{DS}) greater than 30 V to 40 V. This specification precluded the use of a simple parallel combination of VJFETs in the application.

Investigation Using Back-to-Back VJFETs

After the NGC VJFET asymmetries were characterized, the parts still offered advantages over MOSFETs in a back-to-back configuration. Compared to MOSFETs, VJFETs offer higher operating temperatures due to the absence of an oxide layer. Present VJFETs also have lower on-state resistances for a given chip area. Finally, VJFETs have significantly lower gate capacitances resulting in faster transition speeds.

ARL personnel began evaluation of the parts in a simple test setup. Two 8 A VJFET parts were connected in a back-to-back configuration with common sources, like the MOSFETs shown in figure 2. The bi-directional snubber shown in figure 3 was connected across the parts. An isolated DC power supply was used as a source, and a 50 ohm load was connected in series with the VJFETs as shown in figure 7. The setup allowed the connections of the VJFET pair to be

easily reversed for bi-directional testing. The driver was connected with the gate line to the gates of both VJFETs through individual 5 ohm resistors, and with the source line connected to the common source of both parts.

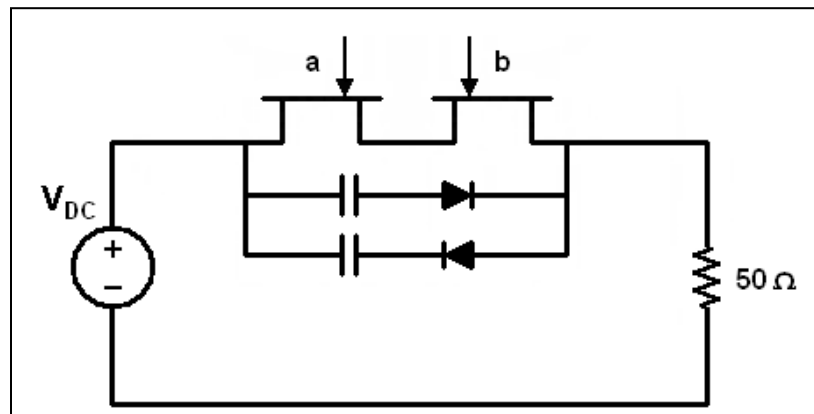


Figure 7. Back-to-back VJFET test configuration.

For each test, the parts were initially held in the off-state at a V_{GS} of -20 V. A single gate pulse of $+2$ V was used to bias the parts to the on-state for 5 ms, after which, the gate bias was returned to -20 V. This test method was used for supply voltages ranging from 50 V to 250 V, in 50 V increments. Figures 8 and 9 show: V_{GS} (ch1), voltage drop across both devices (ch2), and device current (ch3) waveforms for the VJFET configuration tested in both directions for a supply voltage of 100 V.

As indicated by figures 8 and 9, tests run up to and including the 100 V supply voltage showed symmetric bi-directional behavior. However, for tests run in either direction using supply voltages of 200 V and above, a gate-to-source bias of below -20 V was seen at the device turn-off transition as shown in a figure 10. After additional capacitance was added to the -20 V rail of the driver, tests were repeated to show similar behavior. In discussions with NGC, it was determined that device damage could possibly result from the reverse conducting VJFET reaching an off-state more quickly than the forward conducting VJFET.

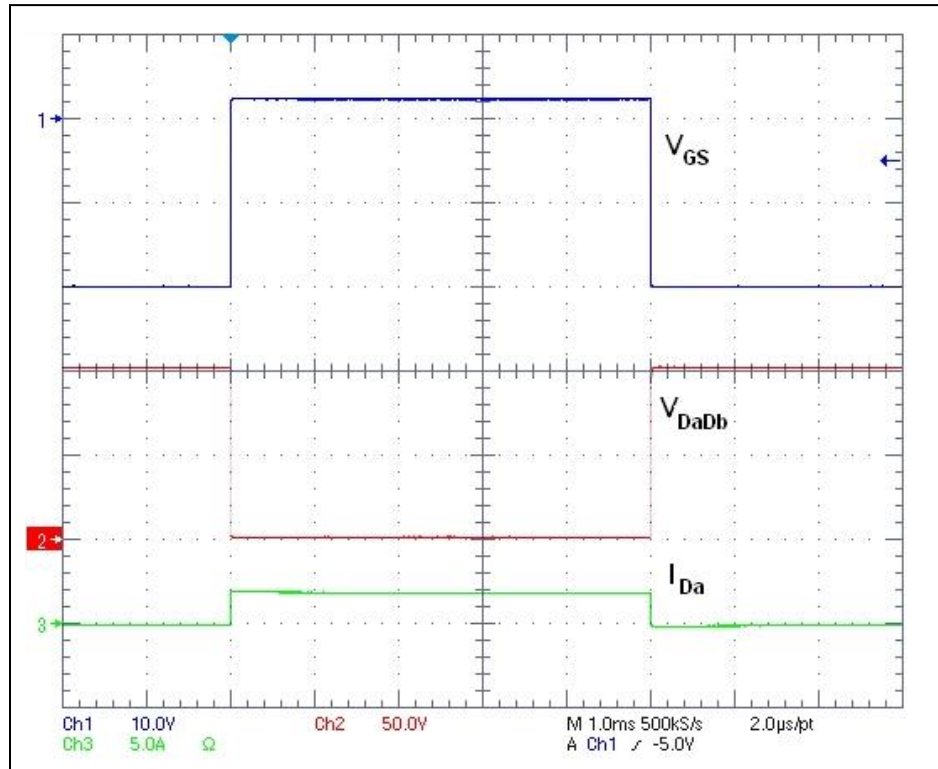


Figure 8. Back-to-back 100 V, 5 ms, VJFET test (part **a** drain connected to positive of supply).

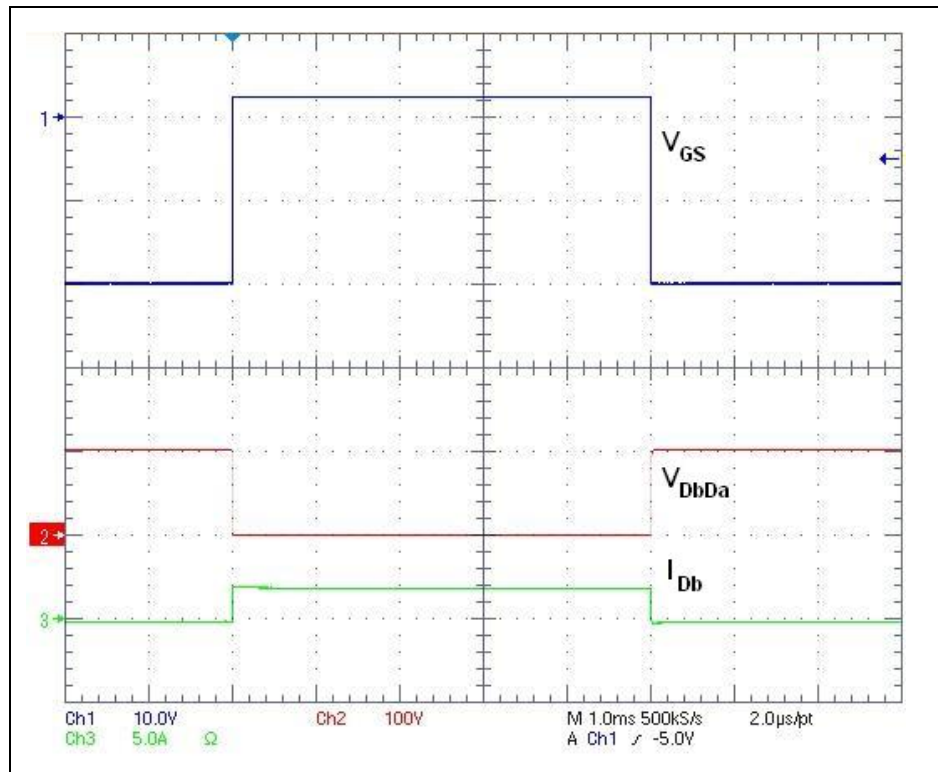


Figure 9. Back-to-back 100 V, 5 ms, VJFET test (part **b** drain connected to positive of supply).

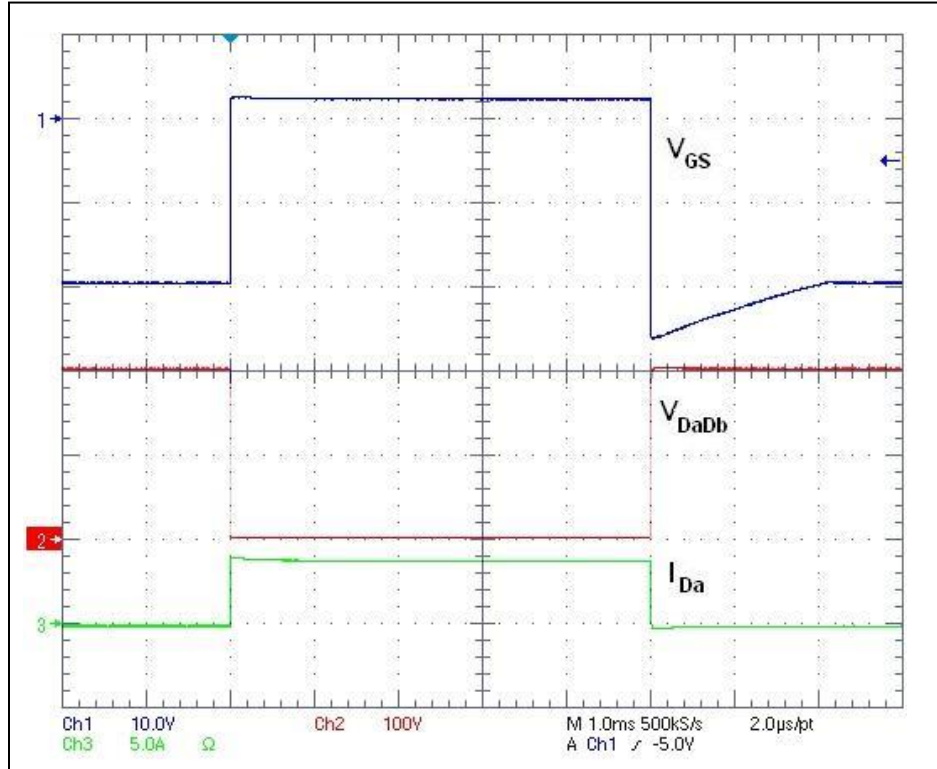


Figure 10. Reduced V_{GS} at turn-off during tests using supply voltages at or above 200 V.

To address the issue, a second gate driver stage was added to the existing design to provide a delayed turn-on signal to the device in position to forward conduct (or voltage block). This same device was also provided a turn-off signal before the reverse conducting (or non-blocking) device. Gate signal delays are shown in figure 11.

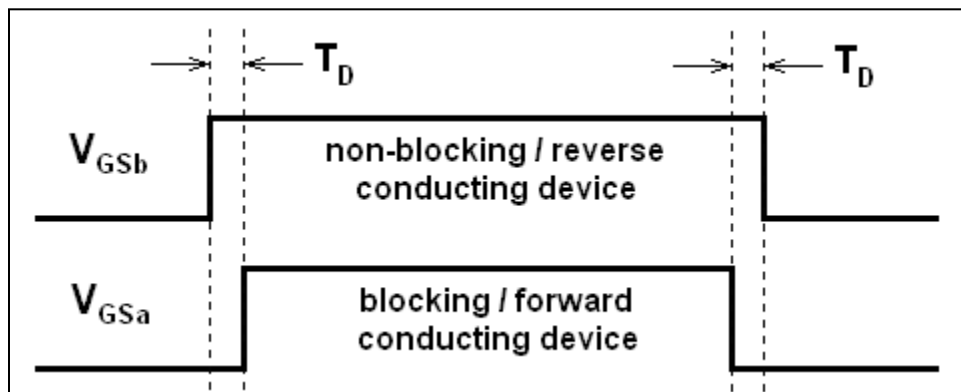


Figure 11. Gate signal delays for turn-on and turn-off of back-to-back VJFETs.

The parts were re-tested with delays ranging from 2 μ s to 10 μ s with the same undesired behavior seen on the -20 V gate driver rail during tests in both directions for 200 V or greater supply voltages. After taking additional voltage and current measurements, it was found that the

+2 V rail of the driver was supplying continuous current (tens of mA) to the gate of the reverse conducting device during these tests. The driver was not designed to provide such continuous current to the gate of the device during the on-state. In discussions with NGC, it was determined that the continuous gate current was a result of undesired forward conduction of the parasitic diode having its anode at the gate and its cathode at the drain of the VJFET. The high supply voltages cause larger currents to flow through the VJFETs, resulting in larger voltage drops across the devices. For the reverse conducting device, a negative V_{DS} is established which in conjunction with the V_{GS} of +2 V, forces V_{GD} to be equal to $V_{DS} + V_{GS}$. This effect is illustrated in figure 12.

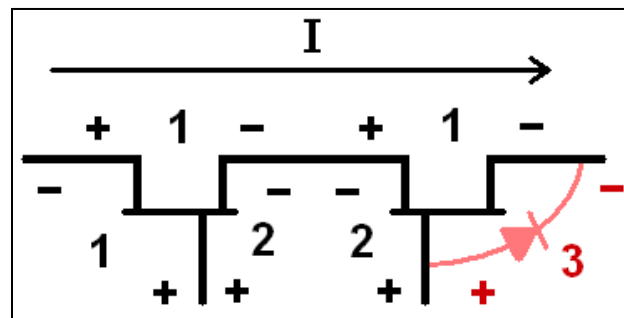


Figure 12. Nominal voltages in VJFET configuration resulting in parasitic diode conduction.

NGC stated that the parasitic diode between the VJFET gate and drain terminals begins to forward conduct at approximately 2.7 V. The voltages between the drain and source terminals of the VJFETs shown in figure 12 correspond to a current of approximately 4 A, which matches up with the load voltage of approximately 200 V divided by a load resistance of 50 ohms. In tests using a supply voltage of 250 V, an increase in the parasitic gate current was seen. The trend is projected to worsen and inhibit proper device operation as reverse conducted current rises. According to NGC, even at low levels of parasitic current, permanent device damage can result from this mode of operation.

Summary

For the back-to-back VJFET configuration to function properly in this application, either a reduced V_{GS} (for at least the reverse conducting device) is required, or enough pairs of devices must be connected in parallel to keep the voltage drop between the source and drain of the reverse conducting device below 1 V. In either case, these actions would effectively de-rate the devices by nearly a factor of 2, causing almost twice as many back-to-back device pairs to be required for a given current level. To apply a reduced on-state V_{GS} to only the reverse

conducting device would also increase gate driver complexity, in addition to the sensing and conditioning needed to determine current direction for sending proper gating delays. Not to increase driver complexity, by applying the same reduced on-state gate voltage to both devices, would result in unnecessary additional losses. Even if enough device pairs were used for a rated current, the resulting solid-state breaker would have instability at current levels above the rating, which could result in component failure. Avoiding the instability would require significantly increasing the number of devices used. This type of instability is not present when using typical semiconductor devices that allow twice rated current, or more, for short durations.

The feasibility of fabricating a custom fully symmetric SiC JFET rated for 1200 V blocking and bi-directional current conduction was discussed with NGC. The device would require an unconventional driver circuit capable of providing gate-to-drain bias and gate to source bias. Although a design study would need to be conducted, device engineers believed the concept to be very realizable. The most obvious drawback to the proposed structure is delayed response times, possibly on the order of one microsecond. Considering the speed of present mechanical contactors, ARL personnel see this drawback as insignificant. No other major disadvantages in thermal conductivity, gate bias levels, voltage blocking capability or otherwise were readily apparent on initial inspection. Although silicon JFETs find extremely few applications in the field of power electronics due to their inherently low-voltage blocking capability, it is important not to underestimate the roles SiC JFETs can fill in this application.

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